Advances in Real Time Digital Signal Processing Systems and Applications

Subramaniam Ganesan

Professor, Department of Electrical and Computer Engineering, Oakland University, Rochester, MI 48309
E-mail: ganesan@oakland.edu

Abstract: This presentation covers advances in real time Embedded DSP processor based systems design and applications. Topics covered include characterizing real-time systems, task scheduling, advances in DSP, VLIW DSP, Davinci DSP, VLYNQ interface, FPGA, SOC, Parallel DSP systems; Research Issues, and Practical applications in military and consumer products.

1. Introduction

Advances in circuit technology, architecture, algorithms and VLSI design techniques have contributed to high performance Digital Signal Processing (DSP) microprocessors and to multitude of novel applications of DSP chips. DSP processors are RISC based which have fast arithmetic units, on chip memory, analog interface, serial ports, timers, counters, facilities for inter processor communications and other special features. History of DSP processors reveal that around 1984 we had DSP processors I generation, around 1986 the second generation, around 1988 the third generation and in 1989 RISC processors and 1990 the MISC- minimum instruction set processors. Current high performance DSP processors have VLIW architecture, multiple heterogeneous/ homogeneous cores, high speed interface to co-processors etc.

DSP micros are reduced-instruction-set computers optimized for the fastest possible execution of the following instructions: Addition, Subtraction, Multiplication, Shifting, Single cycle multiplication and shifting using ARRAY multiplier and barrel (or combination) shifter. In contrast, general purpose micros have multiple cycle, micro-code instructions that make use of the ALU’s single cycle, parallel-add, single bit shift capability.

DSP micros employ Pipe lining of instructions, Use of addressing modes that efficiently access relevant data structure (e.g., auto increment, auto decrement modes for arrays & Indexed addressing modes for FFTs) and have dual-bus Harvard architecture which enables simultaneous fetching of data and instructions. special DSP related addressing modes (e.g., Index computation module an arbitrary number, automatic circular queue or free data move for FIR filters, bit reversal for FFTs), extra addressing, Multiple ALUs, special interfaces to serve specific fields of application (e.g., serial interfaces for CODEC in telecommunications) etc. VLIW (Very large instruction word) based TI DSP 6xxx processors can compute up to 8 instructions in one instruction cycle time of 10 ns, since it has multiple arithmetic/functional units.

DSP has the capability to perform floating-point arithmetic including multiply-accumulate operations with an increased degree of parallelism. DSP algorithms are mathematically intensive. Computations require repeated multiplication with coefficient and summation. DSP processor must effectively handle sampled data in large quantities and must be flexible to accommodate changing algorithms, new DSP processors etc. As long as the system samples the analog input at a frequency that is at least twice the information band width of that input, all information present in the original analog signal is contained in the digital signal. A/D conversion introduces quantization noise. Signal to quantization noise ratio or SQNR is a function of A/D’s accuracy. DSP stores current A/D sample and N-1 previous samples in a sample shift register, or a RAM which can simulate shift register function by modifying memory address pointers. The coefficients are stored in ROM or RAM and they determine the impulse response and filter characteristics. A large N gives a longer impulse response and generally produces filters with sharper roll-off, greater stop band attenuation, and less frequency ripple. Some DSP applications involve sampling rates of up to 100 Mhz and 100 MIPS. Linear system obeys the principle of superposition. If an input consisting of a number of signals...
is applied to a linear system, then the output is the sum or the superposition of the system’s responses to each signal considered separately.

If we apply a complicated signal containing many frequencies, the output must be the sum of output due to each input frequency, considered separately. The output contains only those frequencies present in the input. Time Invariant system is the one whose property do not vary with time. LTI, Linear Time Invariant system, has associative property and it means that we may analyze a complicated LTI system by breaking down into a number of simpler subsystems. Commutative Property means that the subsystems can be arranged in series or cascaded in any order without affecting the overall performance. In causal system the output depends only on the present and or/previous values of the input. Stable System is one that produces a finite or bounded output in response to the bounded input. Bit Reversed addressing is a special type of indirect addressing. It is used for implementing FFT.

2. Real Time System

Any system where a timely response by the computer to external input/condition is vital is a real-time system. All critical tasks need to be completed with high accuracy within the deadline. Hard Real-Time (RT) System examples are Aircraft, and Nuclear Reactor control. Soft Real-time System examples are Multimedia, and Internet access. Research areas in real time systems cover, Computer architecture, fault tolerant computers, networks, embedded systems, standards, digital communication, operating system clock synchronization, etc. For a normal system the goal is fairness to all tasks and it is met using for example round-robin scheduling. For a RT system the goal is to meet the deadlines for all critical and high priority tasks. Task-Execution time should be predictable in RT system.

Real-time applications are generally not concerned with sheer speed but rather with completing (or starting) tasks at the most valuable times, neither too early nor too late, despite dynamic resource demands and conflicts, processing overloads, and hardware or software faults.

There have been a number of proposals for more powerful and appropriate approaches to real-time task scheduling. All of these are based on having additional information about each task. The most popular is the Rate Monotonic Scheduling (RM), which assigns highest priority for tasks with lowest periods (or deadline). One measure of the effectiveness of a periodic scheduling algorithm is whether or not it guarantees that all hard deadlines are met. To schedule sporadic tasks, consider it as periodic task with period equals minimum inter arrival time of the Sporadic task. For critical tasks with long period, break it to small period tasks to get high priority in RM scheduling algorithm.

Market (7.8 Billion dollars) for DSP is approximately shared by TI (65%); Freescale (12%); AD(3%); NEC (4%); Others(16%). A few DSP chips are described below. (http://www.edn.com/dspdirectory)

3.1 ANALOG DEVICES

Analog Devices’ Blackfin, SHARC, SigmaDSP, TigerSHARC, and ADSP-21xx processors and analog microcontrollers make up the company’s embedded-processing and DSP portfolio, supporting high-speed, multi-DSP signal-processing, converged signal- and control-processing, fixed-function-processing, and microcontroller applications. Development tools for all of the company’s processors include the VisualDSP++ integrated development and debugging environment, EZ-Kit Lite evaluation kits, EZ-Boards evaluation boards, and EZ-Extender daughtercards and emulators, as well as tools from SigmaStudio, and μClinux.

The Blackfin processor family combines a 32-bit RISC-like instruction set with 16-bit dual MAC (multiply/accumulate) units and targets convergent applications with audio-, video-, and data-processing requirements. The 32-bit floating/fixed-point SHARC processor family targets applications ranging from consumer,
automotive, and professional audio to industrial, test-and-measurement, and medical equipment. Analog Devices’ SigmaDSP audio processors provide a single-chip audio system with a 28/56-bit audio DSP, ADCs, DACs, and microcontroller-like control interfaces. Signal-processing elements include equalization, crossover, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo-image widening.

The TigerSHARC processor family offers high floating-point- and fixed-point-performance with glueless multiprocessor scalability to target wireless-communications-infrastructure, medical-imaging, industrial-imaging, and military applications. ADSP-21xx processors are code- and pin-compatible DSPs that operate as fast as 160 MHz and consume as little as 184 µA of power. The ADSP-21xx family is ideal for speech processing and voice-band modems, as well as real-time-control applications.

### 3.2 FREESCALE SEMICONDUCTOR

Freescale Semiconductor designs and manufactures embedded semiconductors for the automotive, consumer, industrial, and networking markets. Freescale offers programmable DSPs based on StarCore technology that target advanced communications and networking-infrastructure equipment. The company also offers advanced 16-bit DSCs (digital-signal controllers) that find use in factory automation; building and lighting control; and a range of motor-control applications, such as large appliances. Freescale’s flagship six-core MSC8156 DSP employs SC3850 StarCore DSP technology to advance the capabilities of wireless-broadband base-station equipment.

### 3.3 TEXAS INSTRUMENTS

Texas Instruments offers a broad portfolio of programmable DSPs. The TMS320C5000 DSP platform offers reduced power consumption and advanced signal processing. The TMS320VC5505 and TMS320VC5504 provide higher integration with low standby and active power for portable medical, biometrics, and audio/voice applications. The TMS320C6000 DSP platform comprises high-performance fixed- and floating-point DSPs. The low-cost, networked TMS320C6743 DSP offers higher system performance, increased on-chip memory, and an integrated MAC (multiply/accumulate) unit for floating-point ease and precision with the efficiency of fixed-point processing. TI also offers the TMS320C6742, TMS320C6746, TM2320C6748, and OMAP (open multimedia-applications processor)-L138 with connectivity options and unique peripherals in a low-cost, low-power format for intelligent occupancy sensors and power-protection systems.

DaVinci video processors include processors, software, tools, and support for developing digital-video applications. The TMS320DM365 processor employs an ARM926EJ-S with an integrated image-signal processor for intelligent video processing and provides multiformat, multirate video with production-qualified H.264, MPEG (Motion Picture Experts Group)-4, MPEG-2, JPEG (Motion Joint Photographic Experts Group), and VC1 (video codec 1) codecs. It targets use in video-security applications. The OMAP35x processors target applications such as portable navigation devices, Internet appliances, and portable patient-monitoring devices.

### 3.4 XILINX

Xilinx offers programmable-logic products. The Xilinx XtremeDSP development-tool package provides a comprehensive design suite that enables you to use The MathWorks’ Matlab and Simulink modeling environments for FPGA design. The XtremeDSP tool package includes both System Generator for DSP and the AccelDSP Synthesis Tool. Together, they form a flexible, integrated, and powerful DSP-development environment for FPGAs. More than 90 DSP building blocks are available for the Simulink modeling environment.

### 3.5 ALTERA

Altera's FPGAs and HardCopy ASICs incorporate features that enable high-performance digital signal processing in a number of systems, including broadcast, communications, medical, military, mobile/wireless, and high-definition...
video. These features include embedded memory blocks, multipliers, processors, and high-speed I/Os and external memory interfaces. Altera also offers tools, IP, reference designs, and development kits to facilitate the development of DSP solutions. Using the company’s DSP Builder tool, designers can go from system definition/simulation using the Simulink environment from The MathWorks to system implementation. The latest version of DSP Builder features the advanced blockset capability which allows timing-driven Simulink synthesis.

3.6 FPGA Vs DSP

FPGAs are making steady improvements in price and performance for the past many years. FPGAs with large number of Cells and soft core processor implementation are available. Hence with clever design, one can implement parallel operations on the logic cells and some serial implementation on the soft core on FPGA. Now FPGA implementations are widespread in many signal processing applications like sonar, radar, image processing and software defined radio. But, DSP processors still dominate and are highly used in the above applications. Floating point does not lend themselves well to FPGA. Matrix inversion is computed faster by DSP, though FPGA computes very fast multiplication and fixed point applications. Power consumption is higher for FPGA than DSP. FPGAs offer an opportunity to accelerate your digital signal processing application up to 1000 times over a traditional DSP microprocessor.

There are reasons why DSP processors are preferred instead of FPGAs. Algorithms developed for DSP processors are not easy to translate to FPGA hardware. FPGA design tools for DSP design are not available. Model based design using Simulink eases the adoption of FPGAs and accelerates Signal processing, computer vision, control and other systems implementation on FPGA (for example on Spartan-6 by Xilinx).

Some of the DSP applications in real time medical (retina analysis), fingerprint analysis, facial recognition, adaptive noise cancellation, audio effect generation, and arc welding will be presented in detail.

4. Conclusion

In conclusion, FPGA, DSP and General purpose processors (GPP) have each their own place determined by the application and customer needs. The technology is advancing very fast with capability for multiple cores and easy design tools. This will lead to easy design with library modules for SOC (system on a chip) as high performance application specific computers.